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Inner DC Link Capacitor Voltage balancing in Five Level Diode Clamped Multilevel Inverter Using Boost Converter

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A B S T R A C T : This paper deals with the problem of capacitor voltage unbalancing arising in the multilevel inverter. This unbalancing leads to the deterioration in the quality of the ac output voltage, unequal voltage stresses across the components and the useful life of various electronic components. This unbalancing of capacitor voltage is being balanced by the use of two level-boost converter. The simulation is being performed in MATLAB Simulink® and this is being analyzed with different loading conditions.

Keywords: Diode-clamped multilevel inverter;switching signal; two level boost converter;LC filter .

1. Introduction

Multilevel inverter finds wide application in generation of high voltage ac output, they are advantageous compared to simple inverter since the output voltage obtained is in staircase form which closely resembles the sinusoidal shape. Also, the voltage stresses across various electronics components is comparatively reduced because of reduced switching losses, lower switching frequency and lower total harmonic distortion. The three popular multilevel inverter topologies well known are classified as diode clamped or neutral point inverter, flying capacitor multilevel inverter and cascaded or H-Bridge inverter [6]. This are being used in various applications such as static- VAR compensation, back to back dc applications and high voltage grid integration. But one of the disadvantage observed in case of diode clamped and flying capacitor multilevel inverter is capacitor voltage unbalancing [6].

It is being observed that the capacitor voltage balancing strategy is only possible if the modulation index value is limited to a value of 0.8 load power factor and 60 % of load across inverter. This limitation could be overcome by use of the additional external dc sources, extra balancing circuit or modification in the switching pattern [1][2][3].

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Nomenclature

TLBC	Two level boost converter
Vo	output voltage
Vi	input voltage
C1, C2.C3, C4	DC link capacitors
D	duty ratio
S1, S2, S3, S4	switches
Ls	energy storing inductor

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To avoid the additional cost involved in employing external balancing circuit many authors suggested modification in the spwm switching pattern but one of the limitation in employing such a strategy was once the technique is employed it could not cope up with multiple problems at a time like common mode voltage cancellation, total harmonic distortion, leakage current. [4][5].

To avoid this limitation additional auxiliary circuit in the form of two-level boost converter is being employed in this paper. The two-level boost converter employed is advantageous over combination of conventional boost converter in the form of reduced inductor size requirement, lower reverse recovery losses, lower conduction losses, the current ripple is halved compared to conventional boost converter[5].

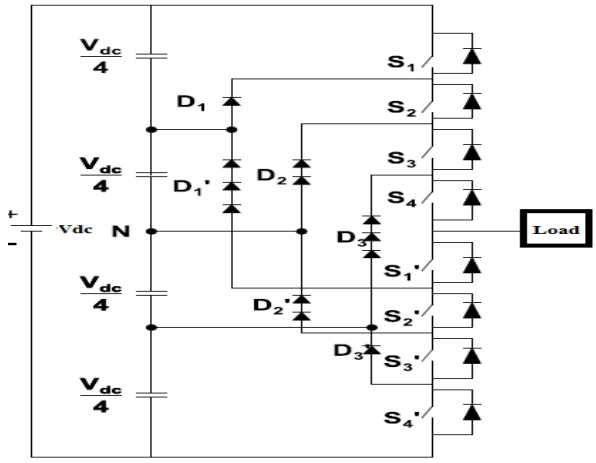

Figure 1 five-level diode clamped multilevel inverter

2. Five-level diode clamped multilevel inverter

Diode clamped inverter or neutral point clamped inverter topology was being introduced in the year 1981 by Nabae et.al.it was basically a three-level inverter comprising of two dc link capacitors providing the two levels and an additional level provided by neutral thus the three-level inverter. Based on the required inverter level configuration the number of devices required is being found out. For a single-phase inverter, no of capacitors required in dc link is given by the (m-1) where m stand for the number of levels, more the levels smoother the output voltage waveform with lower total harmonic distortion. Number of switching devices (2m-1) and (m-1) *(m-2) gives us the required number of clamping diodes [6].

To get the desired ac output voltage the switches are turned accordingly top switches are denoted by Sa_1-Sa_4 and bottom switches by Sb_1'-Sb_4'.

Thus, for getting the required voltage the switches turned on are as explained

1.for voltage=Vdc/2 all top switches are turned on

2.for voltage =Vdc/4 three top and one bottom switches are turned on.

3.for voltage=0 two top and two bottom switches are turned on.

4.for voltage=-Vdc/4 three bottom and one upper switch is turned on.

5.for voltage=-Vdc/2 all bottom switches are turned on.

One of the disadvantage being observed here is unbalancing in the capacitor voltage due to the unequal voltage levels being provide by the switches.

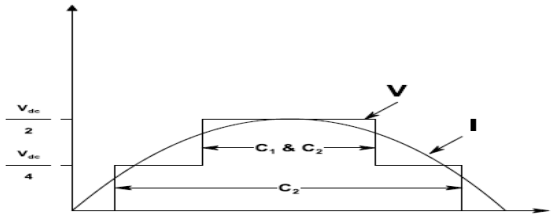

Figure 2 DC capacitor voltage unbalancing

As seen from fig.2 based on the requirement the capacitors are used. Capacitor $C_1$and C_2 are being turned on for supplying the voltage Vdc/2 but as can be seen for supplying the voltage equal to Vdc/4, C_2 continues to discharge but C_1 goes into charging state thus due to this the required amount of current supplied by the C_2 is more leading to more discharging. This voltage unbalancing problem leads to the situation where the multilevel configuration of inverter start behaving as a simple three level inverter. Similar condition exists for C_3 and C_4. This condition exists regardless of load power factor control employed or not. So, for this additional balancing circuit is to be introduced which balances the inner capacitor voltage. Thus, the solution adopted here is two level boost converter.

2.1. Switching of multilevel inverter

The switching strategy adopted here is sinusoidal pulse width modulation strategy [SPWM]. This strategy of switching was being employed for the modulation index of 0.9. It was found that the PDPWM technique gave the value of lower total harmonic distortion of 20.73%.

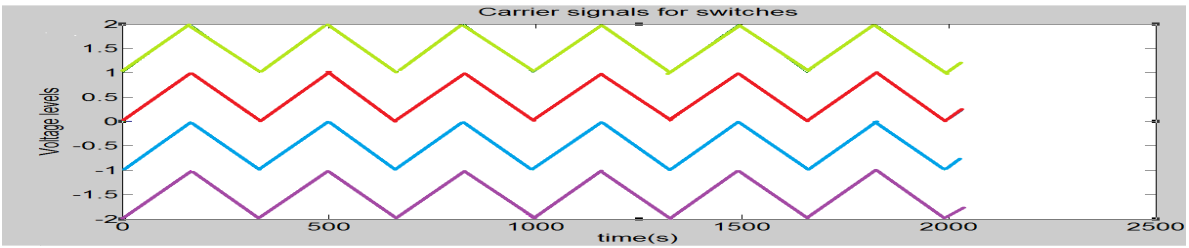

Figure 3 PDPWM switching for inverter

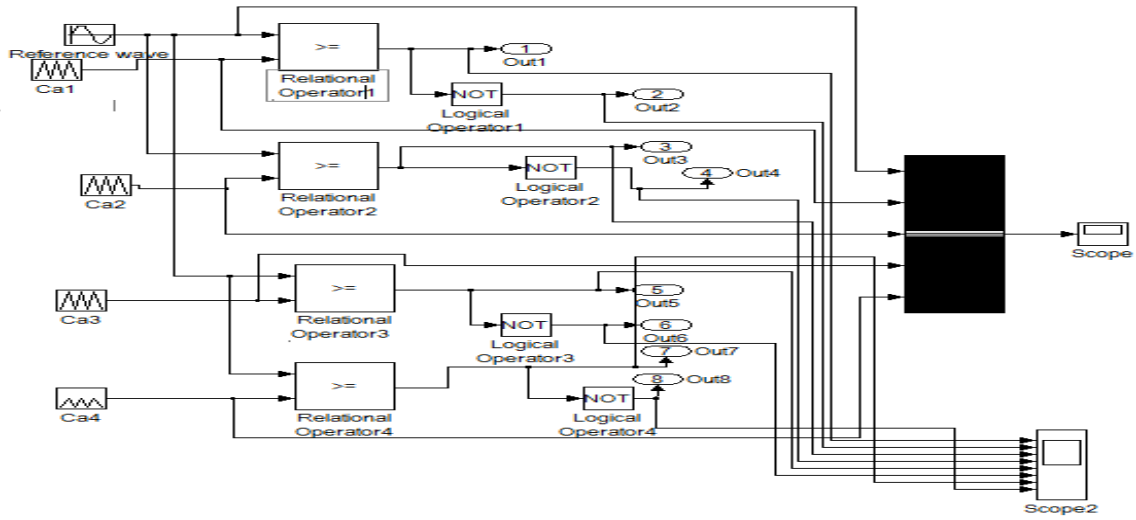

Figure 4 control for the switching signal

3. Two level boost converter

The two-level boost converter circuit is being employed for balancing of the inner capacitor voltage of five-level diode clamped multilevel inverter since they are the one where unbalancing is mostly experienced. Two level boost used here is a modified form over the conventional type of two-level boost converter connected in parallel wherein two separate inductors are needed for each of the circuit therefore in this two- level boost converter the size of the inductor is reduced and there is corresponding reduction in switching losses and size of the components is reduced to half. converter operates in four different modes [5].

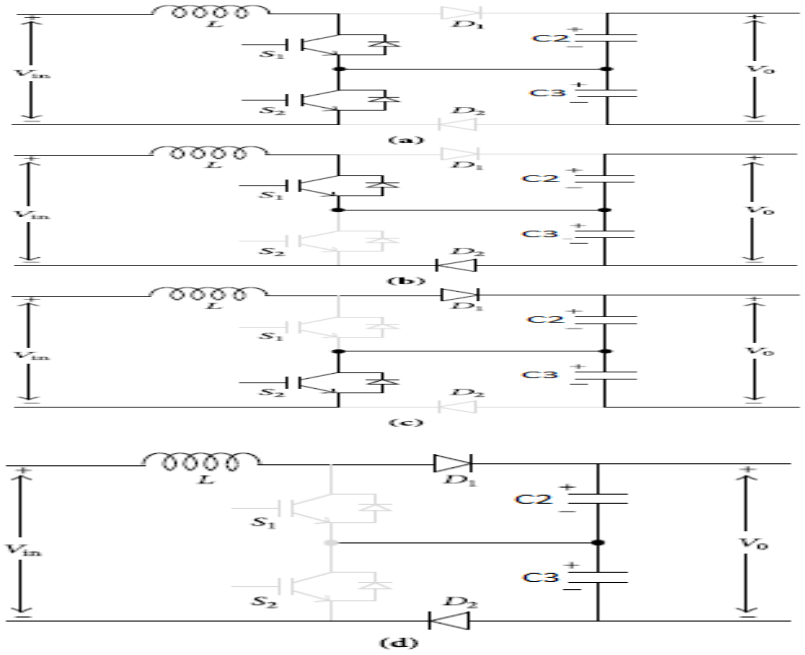

Figure 5 modes of boost converter

As seen from fig.5 the boost converter operates in four different modes. In mode (a), both the switches are turned on and the load is being supplied by the charged capacitors C_2 and C_3 and the inductor continues to charge. In mode (b) S_2 is turned off and the load is being supplied by the capacitor C_2 continues to supply the load. In mode (c) S_2 is turned on and the load is being supplied by capacitor C_3. In mode (d) both switches

$S_1$and S_2 are turned off and the load is being supplied by the supply charging both the capacitors and supplying the load.

The switches $S_1$and S_2 are turned on by such a way that at a time only one of the switch is turned on and the time duration of each other do not overlap with each other. The duty ratio is set to the value of 0.5. This value of duty ratio could be varied between 0 and 1 based on which the amount of charging could be controlled.

The amount of current ripple in the conventional boost converter is given by the equation

$$I=V_s D T_{sw} /L_s \qquad (1)$$

Where Vs is the source voltage, D is the duty ratio, Tsw is the time duration of switching and Ls being the source inductance. The amount of ripple in two-level boost converter is given by the equation

$$I=V_o(1-V_s/V_o)*(2V_s/V_o-1)/2L_sf_{sw} \qquad (2)$$

Where Fsw is the switching frequency of boost converter. From (1) and (2) it can be seen that the amount of current ripple is reduced to half in case of two-level boost converter compared to conventional converter.

4. Simulations and Results

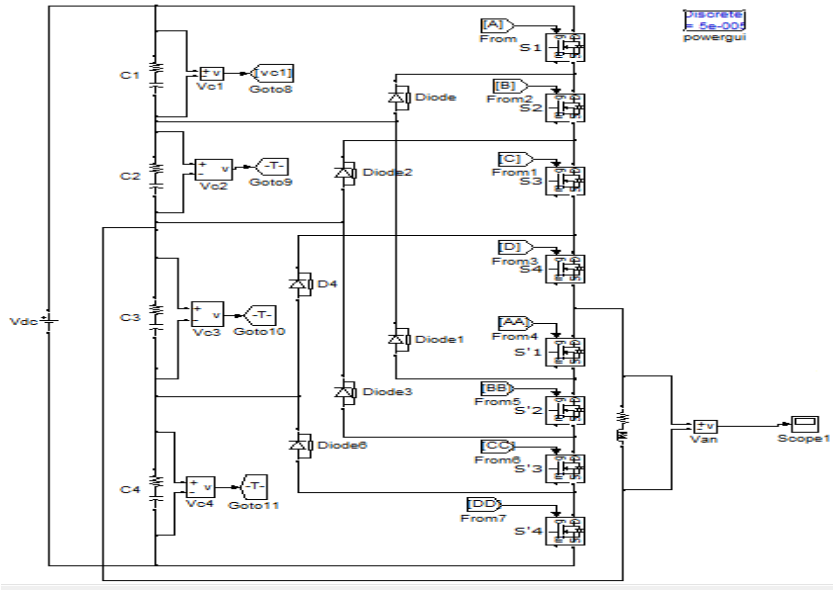

Figure 6 five-level diode clamped inverter

fig.6 shows the five-level inverter having four dc link capacitors and eight switches based on the required output the switches will be turned on and the required voltage levels will be provided by the energy stored in the capacitor. Clamping diodes D_1-D_3 and D_1'-D_3' will operate in order to clamp the voltages.

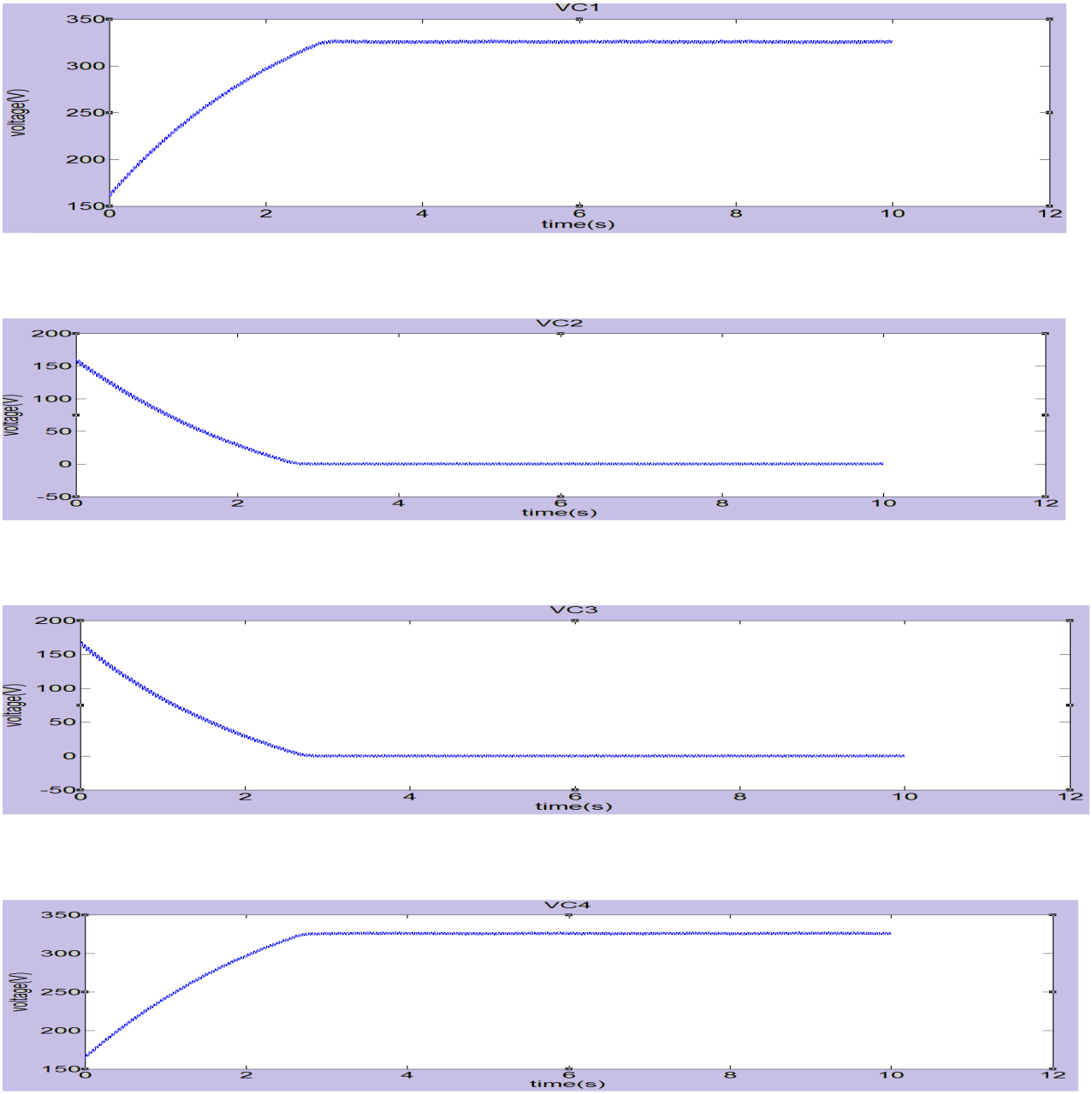

Figure 7 output voltage of capacitors C1.C2, C3, C4

Fig.7 shows us the capacitor voltages here it is observed that the unbalancing is caused due to overuse of capacitor C_2 and C_3. Thus, this voltage unbalancing leads to the conversion of five-level output to three-level output. This unbalancing is being controlled by employing additional auxiliary circuit in the form of two-level boost converter.

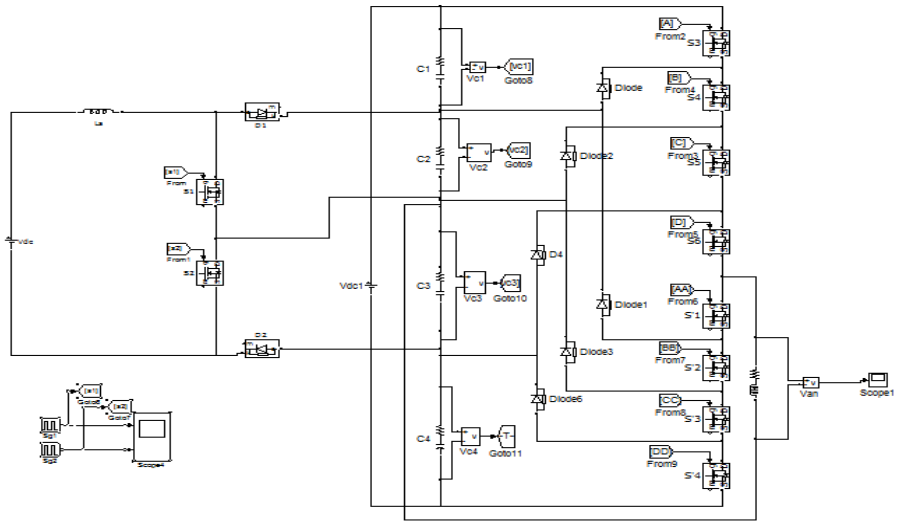

Figure 8 two level boost converter with inverter

Fig.8 shows the two-level boost converter being attached as an auxiliary circuit to balance the inner capacitor voltages C_2 and C_3. The switches S_1 and S_2 are turned on alternately to boost up the capacitor voltages.

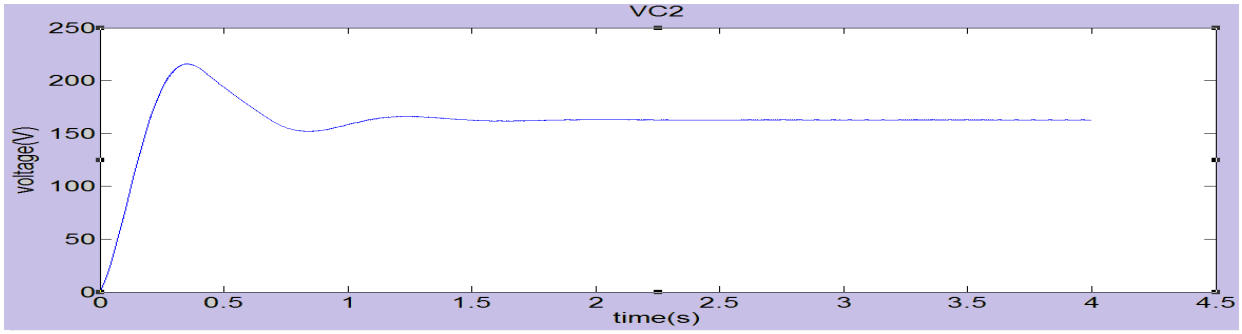

Figure 9 inner capacitor voltage across capacitor C2

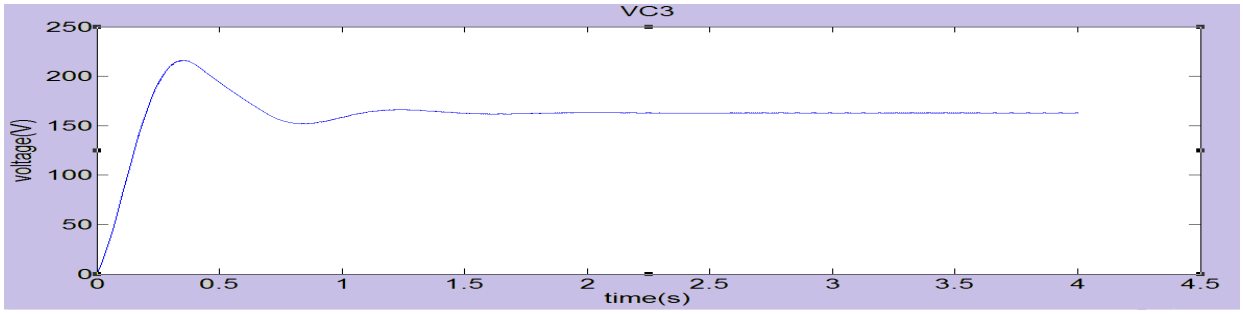

Figure 10 inner capacitor voltage across capacitor C3

From fig 9 and fig 10 we can see the inner capacitor voltage is being balanced by the use of boost converter as auxiliary circuit at the front end of inverter. The inner capacitor voltage balance in being provide for a resistive load of 50 ohm and inductive load of 28.7 milli- henry. Similar condition can be tested for a different value of resistive and inductive load. It is observed that the output voltage of five- level inverter is being maintained uniform due to this additional balancing provided.

5. Table

Sr. No.	Parameters	Value
1	Boost Converter Power Rating	1.1KW
2	DC voltage source Vs	180V
3	DC voltage source Vo	328V
4	DC input voltage for DCMLI	625V
5	Inductance of two level boost converter Ls	9.62mH
6	DC capacitors C_1, C_2, C_3, C_4	2200 microfarad
7	Voltage across dc link capacitors	164V

Conclusion

Thus, the research carried out using boost converter for balancing of the capacitor voltage works well for getting the smooth voltage with lower distortion in output. It is applicable to different loading conditions. Also there is reduction in size of inductor required thus saving the cost.

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